

CMOS-CCD Signal Processor

Description

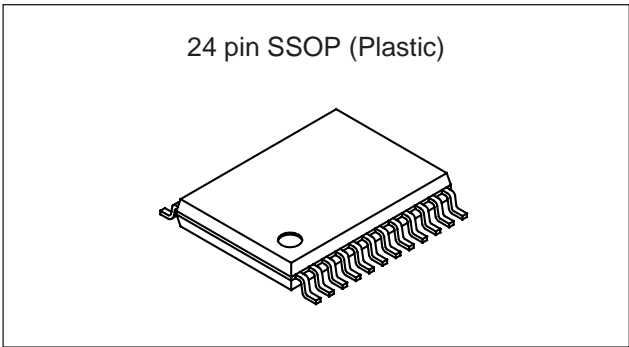
The CXL1517N/1518N are CMOS-CCD signal processors developed for CCD camera complementary color filter array processing system.

CXL1517N

452.5-bit × 2, 453.5-bit 1H CCD delay line

CXL1518N

300.5-bit × 2, 301.5-bit 1H CCD delay line



Features

- Single 5V power supply
- Low power consumption (Typ.)

CXL1517N	120mW
CXL1518N	75mW
- Built-in peripheral circuits
- Built-in CDS (Correlated Double Sampling) circuit

Structure

CMOS-CCD

Functions

- Clock driver
- Autobias circuit (Center and black)
- Pedestal clamp circuit
- CDS circuit
- Overflow prevention circuit

Absolute Maximum Ratings (Ta = 25°C)

- | | | | |
|-------------------------------|------------------|-------------|-------------------|
| • Supply voltage | V _{DD} | 6 | V |
| • Operating temperature | T _{opr} | -10 to +65 | °C |
| • Storage temperature | T _{stg} | -55 to +150 | °C |
| • Allowable power dissipation | P _D | 350 | mW (SSOP package) |

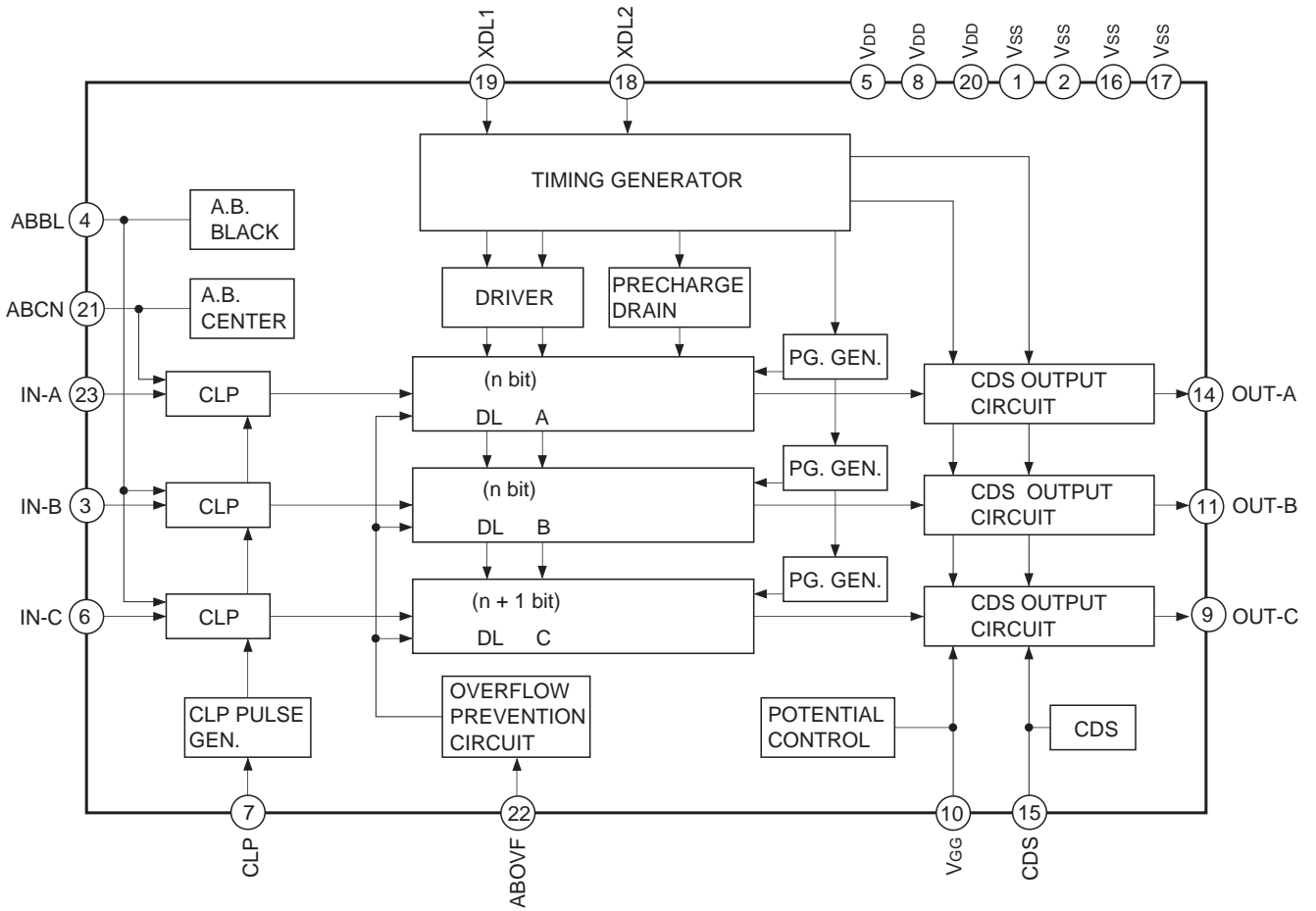
Recommended Operating Voltage Range (Ta = 25°C)

Supply voltage	V _{DD}	4.6 to 5.25	V
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Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock voltage Low	V _L	V _{SS}		0.3 × V _{DD}	V	
Clock voltage High	V _H	0.7 × V _{DD}		V _{DD}	V	
Clock frequency	CXL1517N	f _{CL}	7.16		MHz	NTSC: 455f _H CCIR: 454f _H
	CXL1518N	f _{CL}	4.77		MHz	NTSC: 910f _H /3 CCIR: 908f _H /3

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Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description	Comment
1	V _{SS}	—		
2	V _{SS}	—	GND	Analog
3	IN-B	I	Signal input B channel (Y)	
4	ABBL	O	Autobias DC output for Y signal	Black level bias
5	V _{DD}	—	Power supply	Analog
6	IN-C	I	Signal input C channel (Y)	Black level bias at no clamp > 100k
7	CLP	I	Clamp pulse input	> 100k
8	V _{DD}	—	Power supply	Output circuit
9	OUT-C	O	Signal output C channel	
10	V _{GG}	O	Output circuit bias DC output	
11	OUT-B	O	Signal output B channel	
12	NC	—	—	
13	NC	—	—	
14	OUT-A	O	Signal output A channel	
15	CDS	O	DC output for CDS	
16	V _{SS}	—	GND	Output circuit
17	V _{SS}	—	GND	Timing
18	XDL2	I	Clock pulse input 2	> 100k
19	XDL1	I	Clock pulse input 1	> 100k
20	V _{DD}	—	Power supply	Timing
21	ABCN	O	Autobias DC output for C signal	
22	ABOVF	O	Autobias DC output for overflow prevention circuit	
23	IN-A	I	Signal input A channel (C)	Center level bias at no clamp > 100k
24	NC	—	—	

Electrical Characteristics

Ta = 25°C, VDD = 5.0V, VSS = 0V fCL = 7.16MHz (CXL1517N)
fCL = 4.77MHz (CXL1518N)

Item	Symbol	Test point	SW conditions				Bias conditions	Conditions	Ratings			Unit
			SW1	SW2	SW3	SW4 to 6			Min.	Typ.	Max.	
Autobias center level	ABCN	V1	a	b	a	a	E1		4.2	4.6	4.8	V
Autobias black level	ABBL	V2	a	b	a	a			3.9	4.3	4.5	V
Overflow prevention circuit Autobias level	ABOVF	V3	a	b	a	a			2.6	3.0	3.3	V
CDS source level	CDS	V4	a	a	a	a			1.2	2.3	3.5	V
Output circuit bias level	VGG	V5	a	a	a	a			0.3	0.8	3.0	V
Current * supply	IDD	A1	b	a	a	a	V1		—	24	35	mA
			a	a	a	a			—	15	25	
Insertion gain	IG	V6	b	b	a	a	A → V1 B, C → V2 + 0.25V	20 log $\frac{\text{Output amplitude (mVp-p)}}{\text{Input amplitude (SIN 100kHz, 100mVp-p)}}$	—	—	—	dB
			b	b	a	a			—4.5	—3.5	—	
Frequency * response	fG	V6	b	b	a	a	↓	20 log $\frac{\text{Output amplitude (SIN 1MHz, 100mVp-p)}}{\text{Output amplitude (SIN 100kHz, 100mVp-p)}}$	—1.5	—0.4	—	dB
			↓	↓	a	a			—1.8	—0.8	—	
Linearity	Lin.	V6	b	b	a	a		Note 1)	0	5	12	%
The insertion gain difference between channels	ΔG							Note 2)	0	5	12	%
Linearity difference between channels	ΔLBC							Note 3)	0	1	5	%
Cross-talk between channels	CRT	V6	b	b	a	a	A → V1 B, C → V2 + 0.25V	Note 4)	0	1	3	%

* Standard values are different between CXL1517N and CXL1518N.

Notes)

1) Linearity testing

For A channel, set input bias to ABCN – 0.2V first, and then set it to ABCN and ABCN + 0.2V. Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes. For B channel and C channel, set input bias to ABBL + 0.45V first, and then set it to ABBL + 0.25V and ABBL + 0.05V. Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes. The maximum output amplitude for the respective A, B and C channels is taken as Sout max and the minimum output amplitude as Sout min. The linearity of the respective channels is defined as:

$$\text{Lin.} = \frac{\text{Sout max} - \text{Sout min}}{\text{Sout max} + \text{Sout min}} \times 200 \text{ [%]}$$

2) Calculation of insertion gain difference

As the maximum insertion gain among A, B and C channels is taken as Gmax and the minimum as Gmin, the insertion gain difference between channels ΔG as:

$$\Delta G = \left| 1 - 10 \left(\frac{\text{Gmax} - \text{Gmin}}{20} \right) \right| \times 100 \text{ [%]}$$

3) Calculation of linearity difference

Define B channel linearity as LB and C channel linearity as Lc we obtain the difference ΔLBC as:

$$\Delta L_{BC} = |L_B - L_C| \text{ [%]}$$

4) Cross-talk calculation

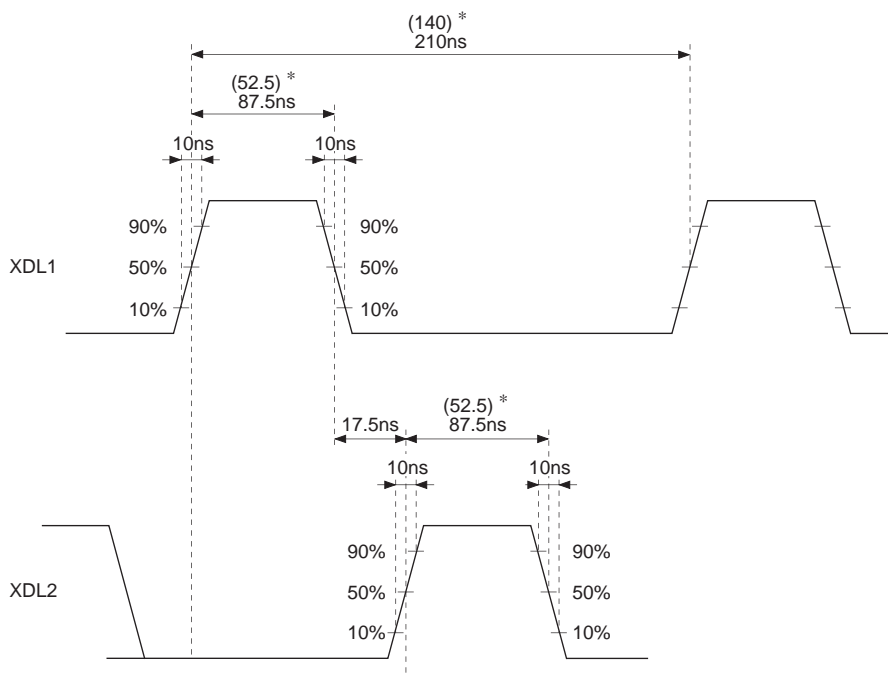
CRTa : The cross-talk value of A channel when B and C channels are input

OUT_{A-a} : The output value of A channel when A channel is input
SW3-a, SW4-a, SW5, 6-b

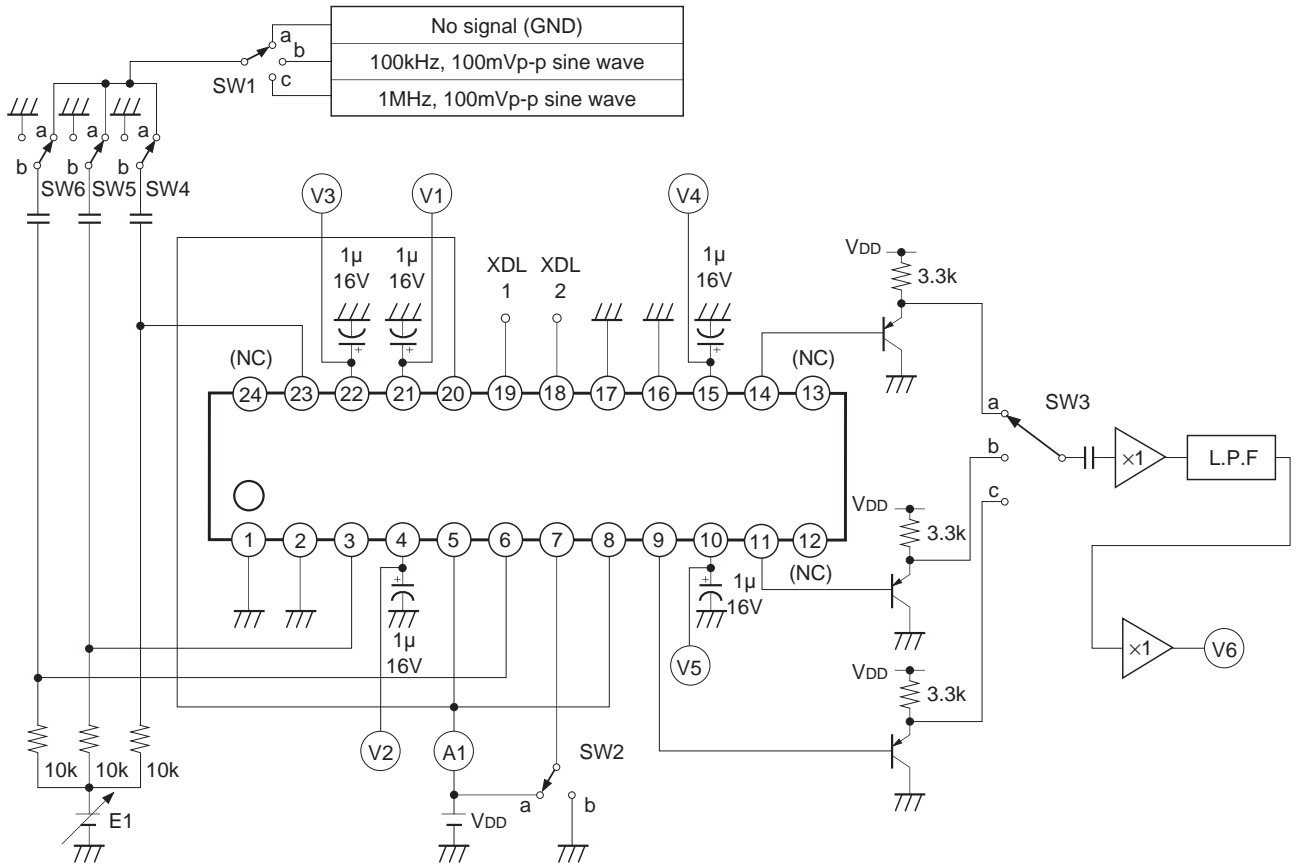
OUT_{A-bc} : The output value of A channel when B and C channels are input
(Cross-talk component)
SW3-a, SW4-b, SW5, 6-a

$$\text{CRTa} = \frac{\text{OUT}_{A-bc}}{\text{OUT}_{A-a}} \times 100 \text{ [%]}$$

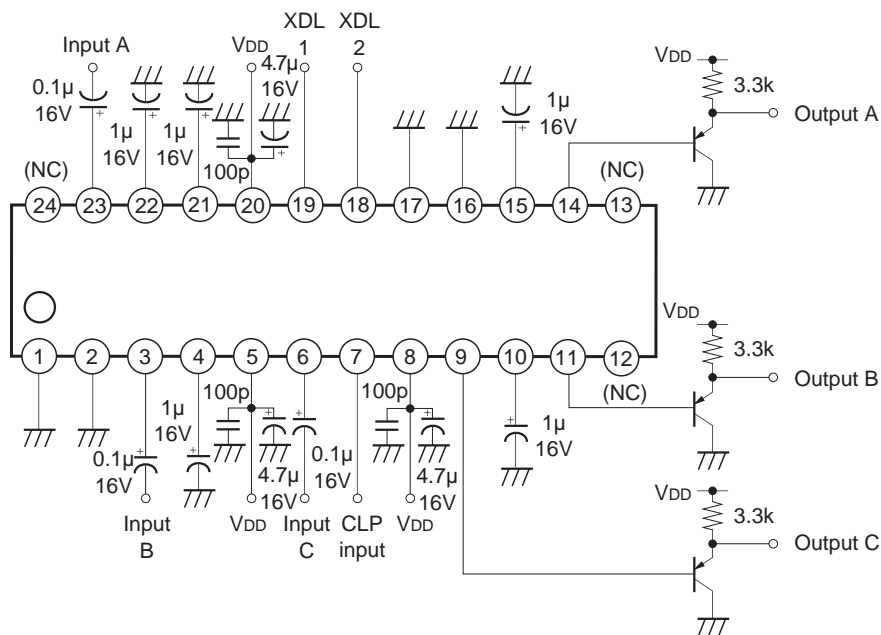
Clock Waveform Timing



Electrical Characteristics Test Circuit



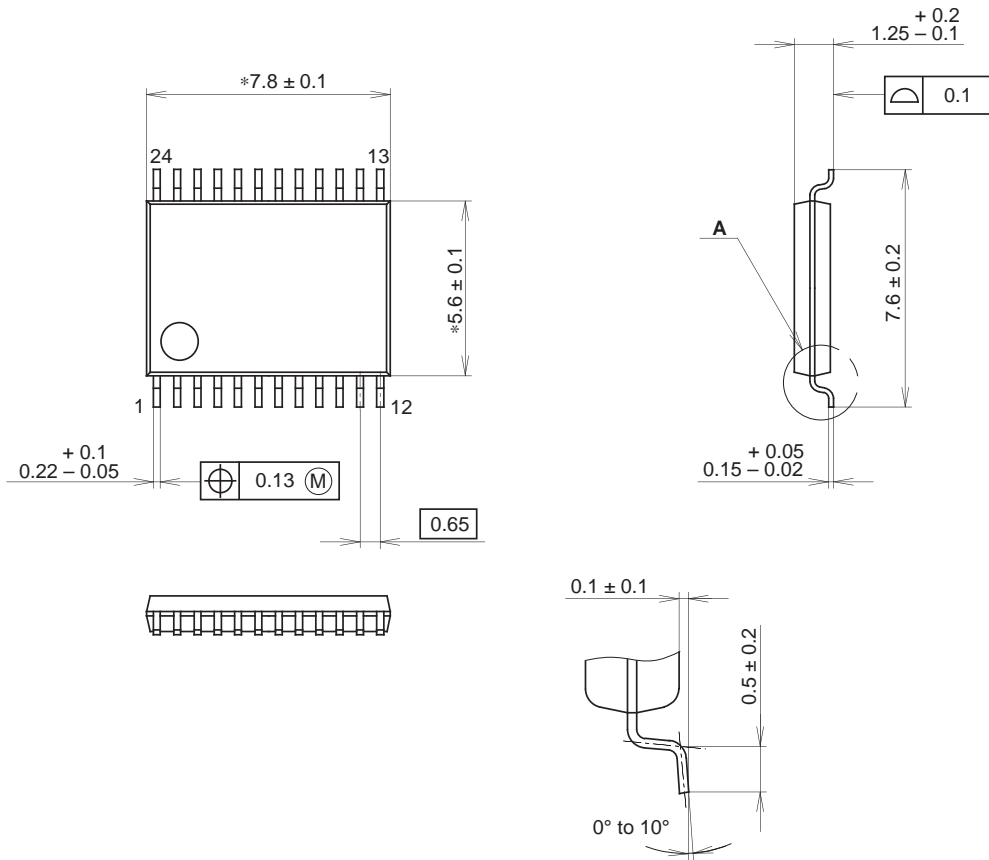
Application Circuit



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Package Outline Unit: mm

24PIN SSOP(PLASTIC)



NOTE: Dimensions "*" does not include mold protrusion.

DETAIL A

PACKAGE STRUCTURE

SONY CODE	SSOP-24P-L01
EIAJ CODE	SSOP024-P-0056
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g