Product Flyer

FUJITSU

# MB86680B
ATM Switch Element (SRE)

The Fujitsu MB86680B is a Self-Routing switch Element for use in ATM switch fabrics.

The device is organized as a 4 x 4 switch with separate input and output ports running at 155Mbps for matrix expansion. The switch element has non-blocking inputs with a 75 cell buffer per output port. Multiple devices can be used to build larger switch fabrics.

The device is suited to applications in a variety of customer premises equipment such as ATM hubs and network access controllers.

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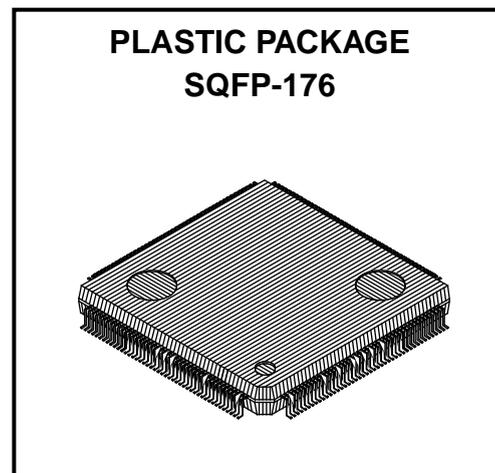
FEATURES

• Highly integrated 4x4 structure

• Active matrix expansion ports for row and column interconnect

• Selectable high and low priority output queues

• Output port buffer capacity of 75 cells, which can be divided into a 50 cell low priority queue and a 25 cell high priority queue

• Multicast support

• Selective cell discard based on CLP bit and selectable queue level

• Selectable Forward Explicit Congestion Notification (FECN) function

• Flexible tag processing to allow a variety of switch fabric architectures to be realized

• All input / output ports operate at up to 20MHz using an 8-bit data format

• Separate input clock signals for each interface

• Separate cell synchronization signals for each port

• JTAG pins compliant to IEEE1149.1 are provided

• Fabricated in 0.8 micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply

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Regeneration Ports

Output Holding Registers

Configuration Manager

Expansion Ports

Expansion Port Holding Registers

Address Filter

MUX

Input Port Holding Registers

JTAG

JTAG Interface

Input Ports

M U X — 75 Cell Output Buffer — Buffer Timing & Control

M U X — 75 Cell Output Buffer — Buffer Timing & Control

M U X — 75 Cell Output Buffer — Buffer Timing & Control

M U X — 75 Cell Output Buffer — Buffer Timing & Control
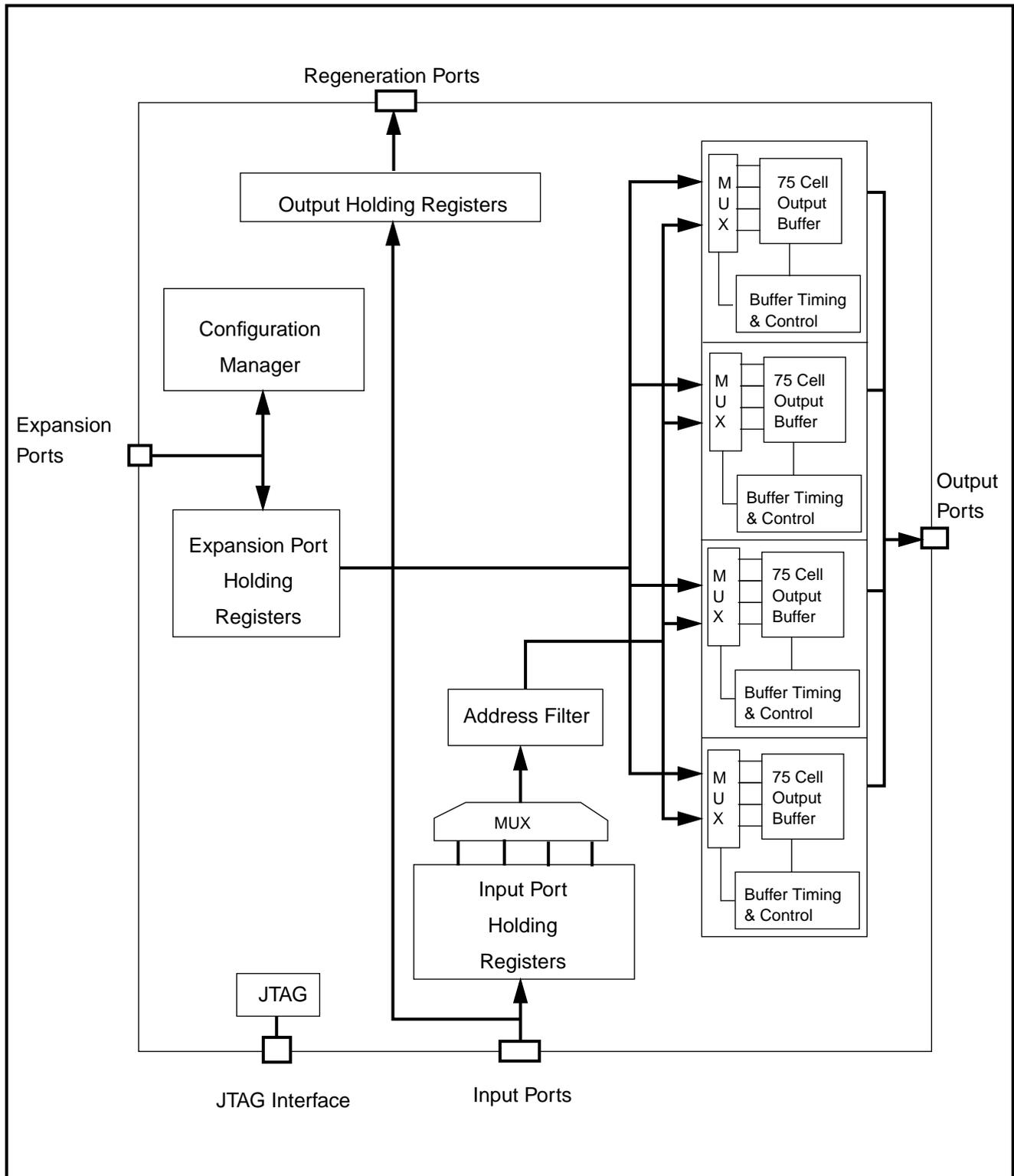
Output Ports

Fig. 1 - MB86680B Block Diagram

MB86680B ATM Switch Element (SRE)

General

The SRE is offered as a basic building block suitable for the construction of a variety of ATM switch fabrics. The SRE provides an aggregate 75 cell storage capacity per port. A flexible output queue configuration permits the allocation of a separate 25 cell High priority queue per port suitable for CBR traffic. On chip Explicit Forward Congestion Indication (EFCI) mechanisms permit early indication of congestion within the switch fabric.

The pin assignment on the SRE minimises the interconnect and real estate required for larger switch configurations.

Traffic Routing

Flexible variations of a 3 byte routing tag appended to the 53 byte ATM cell permit the SRE to carry out Point to Point and Point to Multi-Point (Multicast) connections. Variants of the 3 byte routing tag permit the cell to be marked as a High priority cell or as a Low priority cell subject to selective cell discard.

The selective cell discard feature allows traffic congestion within the switch fabric to be alleviated by carrying out the selective discard of Low priority cells.

The format of the SRE's routing tag permits larger switch fabrics to be constructed without the need for further address translation being required.

EFCI operation

Traffic congestion within individual switch elements may be signalled by the selective marking of the Congestion Indication (CI) bit in the ATM cell's Payload Type (PT) field.

JTAG

The SRE provides boundary scan test circuitry fully compliant with IEEE 1149.1 (JTAG). The SRE's JTAG circuitry permits easier board level testing to be carried out by allowing the signal pins on the device to form a serial scan chain around the device. JTAG test modes are controlled by accessing an internal test access port controller, which is in turn controlled by the 4 provided test access ports.

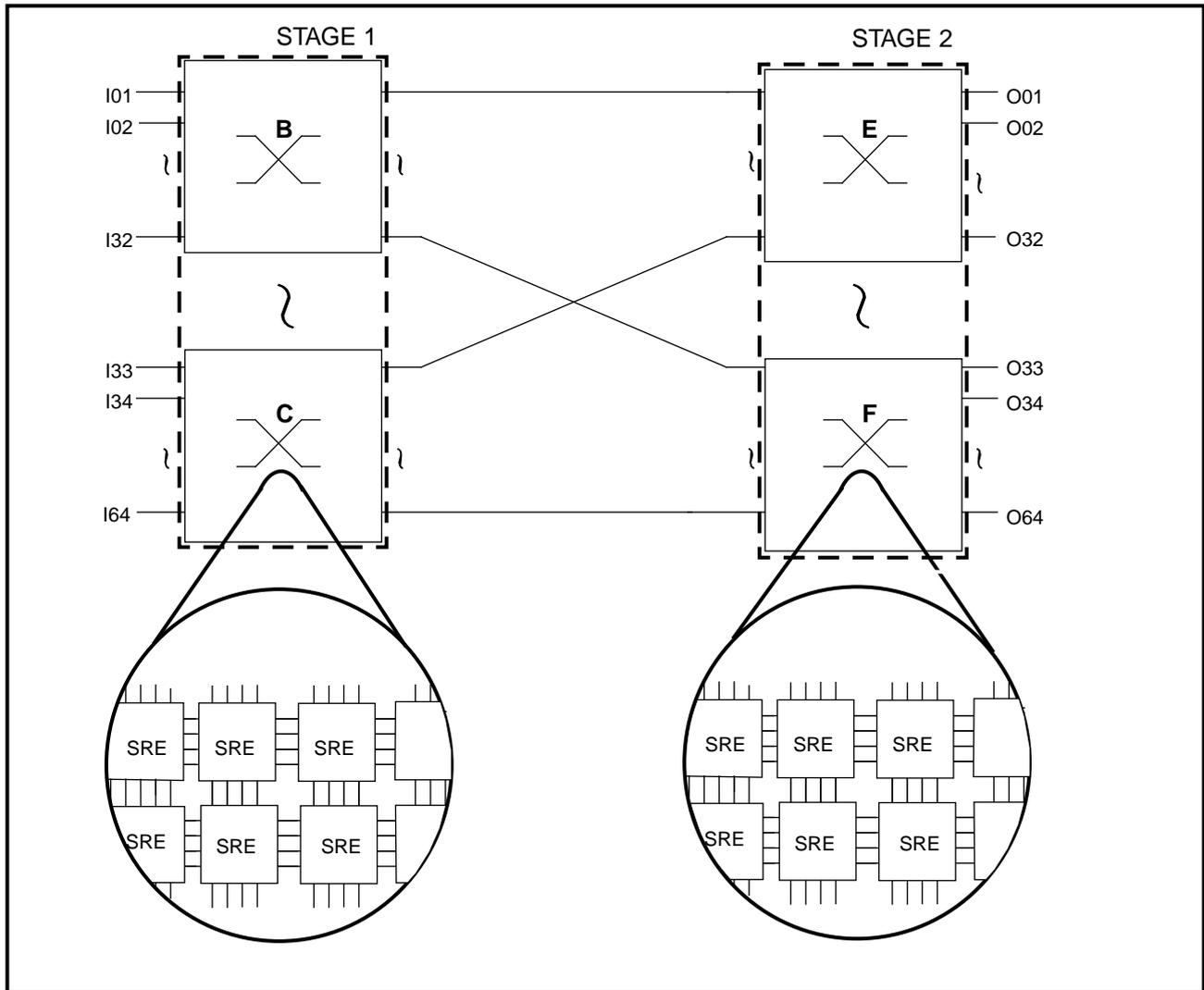**FUJITSU**

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Fig. 2 - Example of a large switch configuration
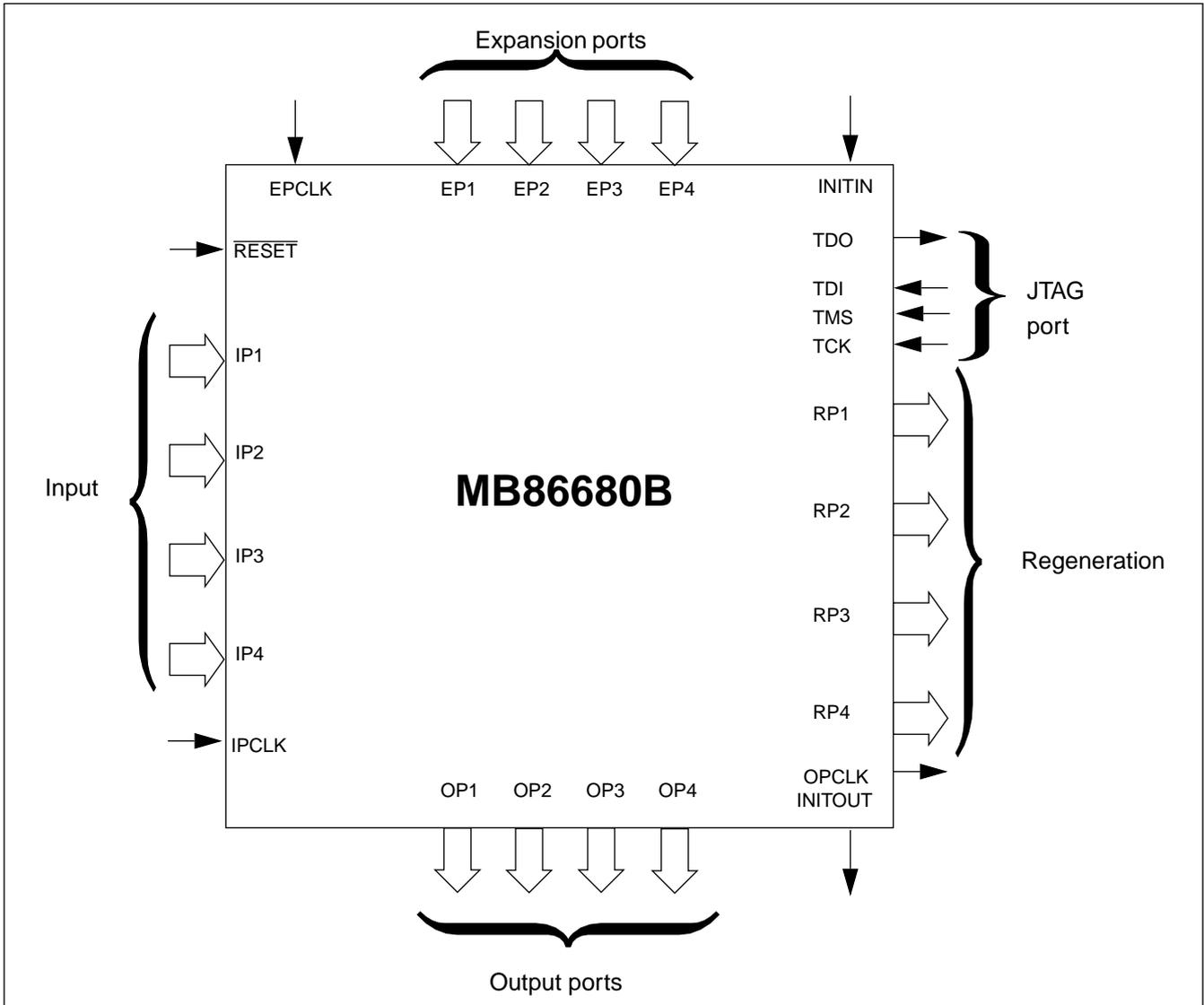
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Expansion ports

EPCLK   EP1   EP2   EP3   EP4   INITIN

RESET

TDO

TDI
TMS   JTAG port
TCK

IP1

IP2

Input   **MB86680B**   RP1

IP3   RP2   Regeneration

IP4   RP3

IPCLK   RP4

OP1   OP2   OP3   OP4   OPCLK
INITOUT

Output ports

Fig. 3 - MB86680B I/O Block Diagram

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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