Product Flyer

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MB86689A

Address Translation Controller (ATC)

The Fujitsu MB86689A Address Translation Controller provides an autonomous high speed translation function of ATM cell header information in real time at 155Mb/s. It replaces ATM virtual path identifiers (VPI) and virtual channel identifiers (VCI) and can append a 1-3 byte routing tag if required.

The device can be used with the MB86683B Network Termination Controller (NTC) or placed directly in the cell stream. When used with the NTC, ATM cell headers are received and transmitted through a dedicated port. When used in the cell stream, ATM cells are received and transmitted through 8-bit parallel cell stream interfaces.

The ATC is ideally suited to UNI and NNI applications in ATM hubs, switches and adapter cards.

**PLASTIC PACKAGE
QFP-80**
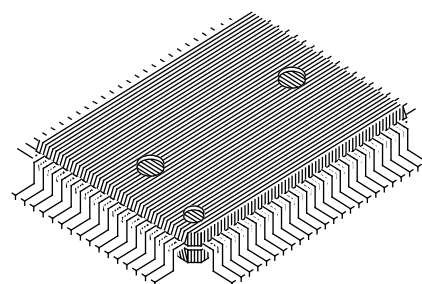
FEATURES

- 1024 entry content addressable memory.
- Full 28 bit comparison for each entry.
- Selectable VPI and VCI mask for each entry.
- Supports UNI and NNI cell header formats.
- Supports multiple matches (NTC Mode only).
- Supports flexible tag sizes.
- Supports the provision of translation data suitable for Usage Parameter Control.
- Supports CLP and congestion indication and removal for each entry.
- Multiple ATCs can be cascaded to support larger translation tables (NTC mode only).
- Translation is completed in less than one cell period at 155Mb/s.
- Entries can be updated on-the-fly without affecting the translation process.
- JTAG pins compliant to IEEE1149.1 are provided.
- Fabricated in 0.8 micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

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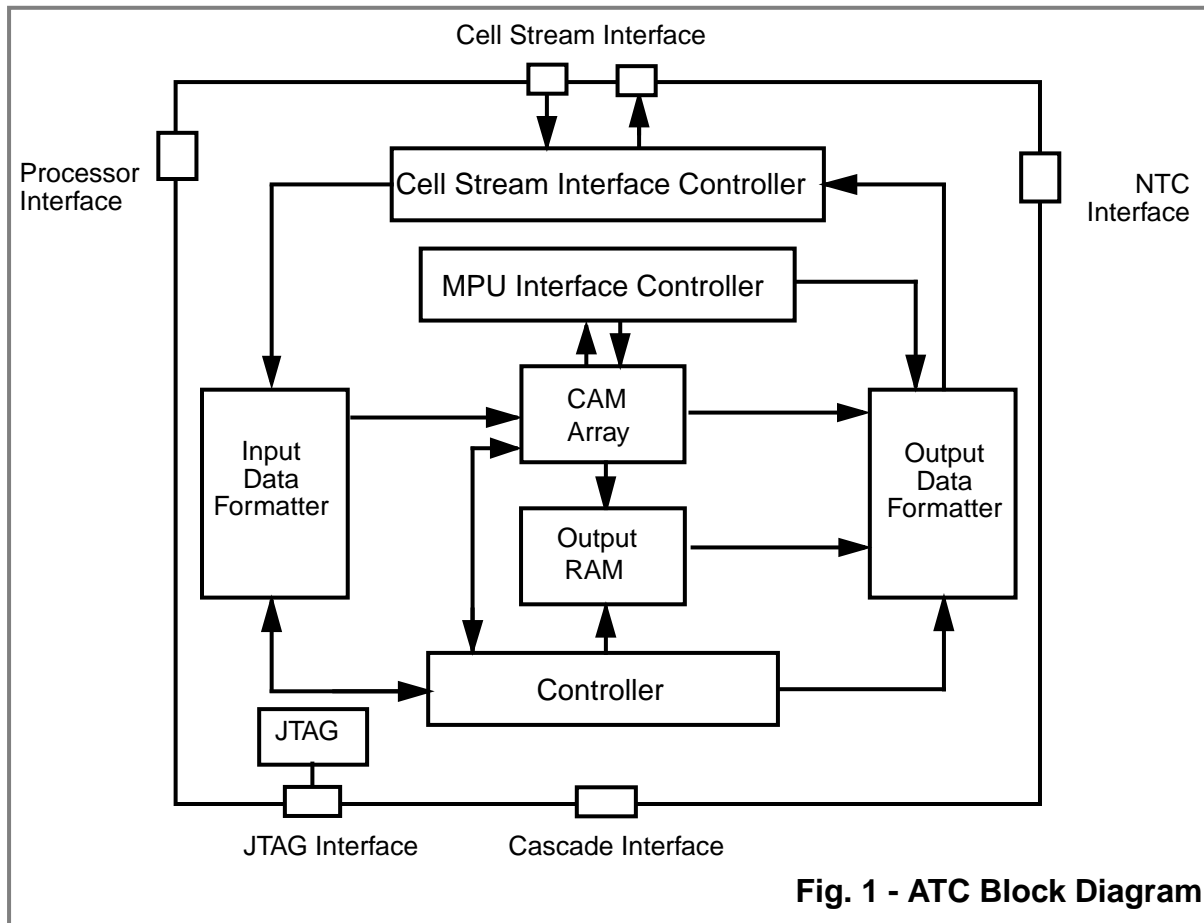# MB86689A Address Translation Controller (ATC)

Fig. 1 - ATC Block Diagram

General

A top level logical block diagram of the ATC is shown in Fig. 1 above. The main modules are as shown and are described below.

The ATC provides high speed translation (<1 cell period at 155Mbps) of header information for 1024 entries, each entry being associated with up to 3 bytes routing tag. The ATC also provides two interface modes; NTC Interface mode and Cell Stream Interface mode. Fig. 2 on page 4 illustrates how the ATC may be configured when the NTC Interface mode is selected and the alternative mode of configuration - Cell Stream Interface mode - enables in-line address translation.

Data Formatters

The Input Data Formatter is responsible for removing an incoming cell's Virtual Path and Virtual Channel Identifiers (VPI and VCI) and for providing this data as a comparend to the ATC's Content Addressable Memory Array (CAM Array). The Output Data Formatter is responsible for providing the newly-translated VPI/VCI data and routing tags for the cell awaiting transmission.

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CAM Array
On receiving the 28-bit VPI/VCI comparend, the ATC compares the data against each active match entry in the CAM Array.

Output RAM
If a match is found between the 28-bit VPI/VCI comparend and an entry within the CAM Array then the ATC activates both the Output RAM and Output Data Formatter. The Output RAM will contain the newly-translated VPI/VCI data and up to 3 bytes of routing tag information.

In NTC mode of operation, if more than one match is detected for the same input data, then the ATC will sequentially output associated RAM data for each match. Multiple matches are not supported within Cell Stream Interface mode.

NTC Interface
This interface allows the ATC to communicate directly with the Network Termination Controller. Transfer of information is across a dedicated bi-directional databus controlled via a 4-wire handshake mechanism. Only header information is transferred across this interface.

Cascade Interface
In NTC Mode, this 3-bit interface allows 2 ATCs to be connected together to form a larger translation table. Each ATC will perform its search in parallel hence incurring no increase in search time. Larger translation tables can be implemented with minimal glue logic.

Cell Stream Interface
This interface allows the ATC to buffer and process entire ATM cells received across a 9-bit cell based interface.

Processor Interface
A 16-bit bi-directional Microprocessor interface allows entries in the CAM Array and Input RAM to be updated on the fly without affecting the translation process.

UPC Port
On detecting a match, the 4-bit UPC port provides a 2-bit ATC code and a 10-bit output RAM address.

JTAG
The ATC provides boundary scan test circuitry compliant with IEEE 1149.1 (JTAG). The ATC's JTAG circuitry permits easier board level testing to be carried out by allowing the signal pins on the device to form a serial scan chain around the device. JTAG test modes are controlled by accessing an internal test access port controller, which is in turn controlled by the 4 provided test access ports.

ATM Terminal Equipment

```
            ┌──────┐
            │ ATC  │
            └──────┘
               │
┌─────────┐  ┌─────────┐  ┌──────────────┐
│MB86687A │→ │MB86683B │→ │ MB582A/583A  │ ←→ □  User Network Interface (UNI)
│  ALC    │← │  NTC    │← │ Transceiver  │
└─────────┘  └─────────┘  └──────────────┘
     │          │
     └────┬─────┘
       ┌──────────┐
       │ Host CPU │
       └──────────┘
```

ATM Switch - UNI Port

```
                        ┌──────┐
                        │ ATC  │
                        └──────┘
                           │
      ┌──────────────┐  ┌─────────┐  ┌──────────┐
UNI □←→│ MB582A/583A  │→ │MB86683B │→ │  Switch  │
      │ Transceiver  │← │  NTC    │← │  Matrix  │
      └──────────────┘  └─────────┘  └──────────┘
                           │
                        ┌──────┐
                        │ ATC  │
                        └──────┘
```

ATM Switch - Signalling controller

```
┌─────────┐  ┌──────┐  ┌──────────┐
│MB86687A │→ │ ATC  │→ │  Switch  │
│  ALC    │← │      │← │  Matrix  │
└─────────┘  └──────┘  └──────────┘
     │          │
     └────┬─────┘
    ┌──────────┐
    │ Host CPU │
    └──────────┘
```
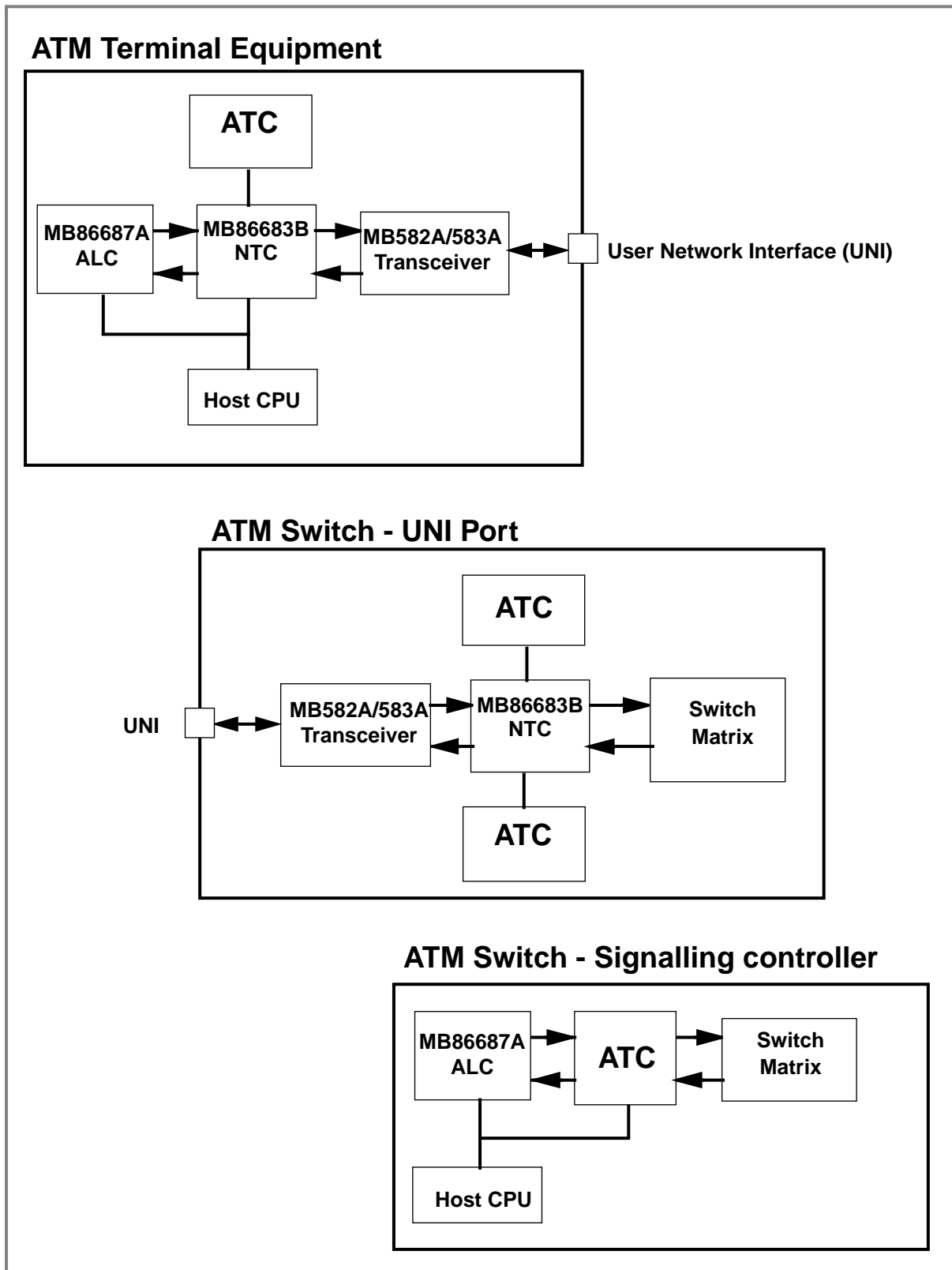
Fig. 2 - Example Configurations

MB86689A Address Translation Controller (ATC)
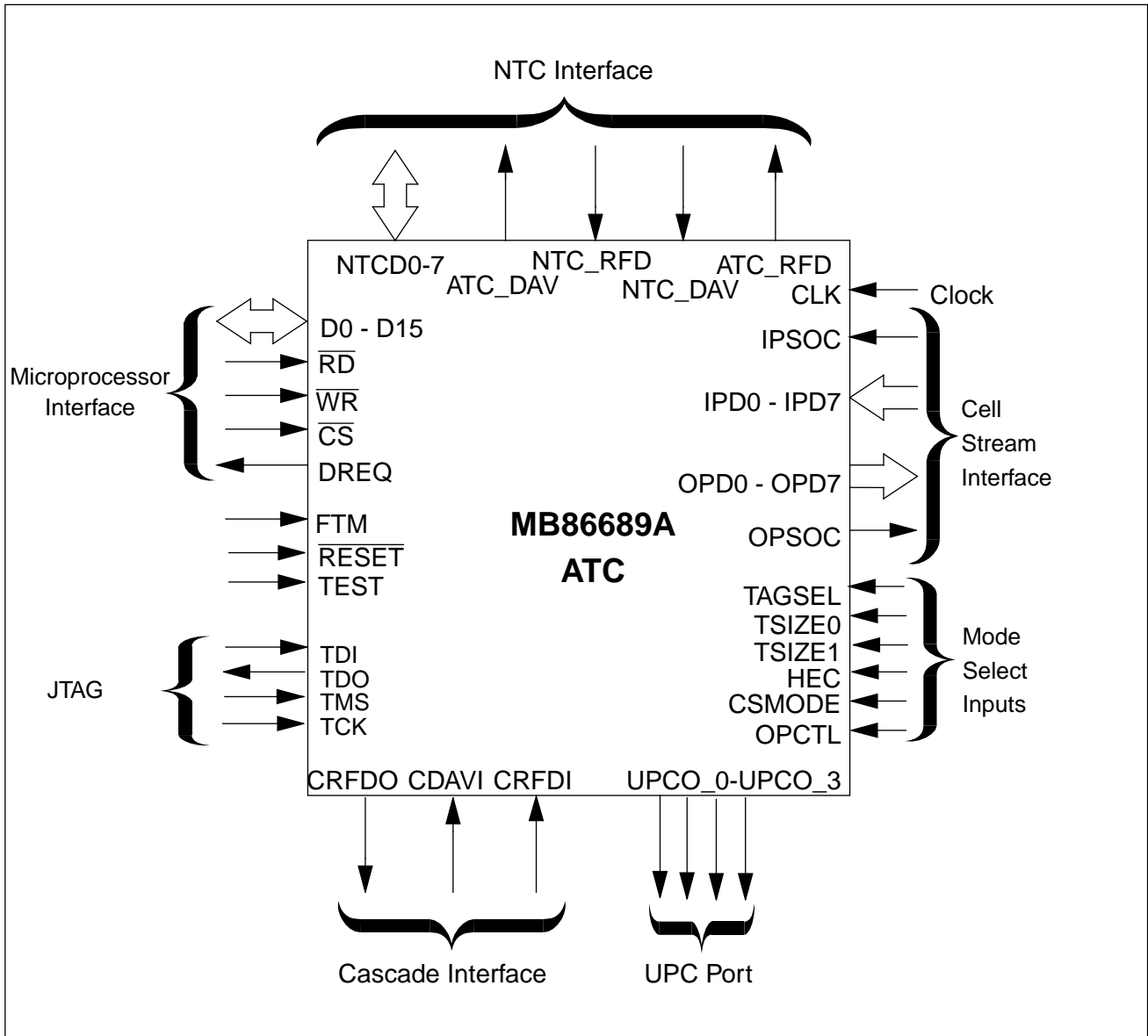
Fig. 3 - MB86689A I/O Block Diagram

MB86689A Address Translation Controller (ATC)

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