

# XC61A

## Series

Low Voltage Detectors ( $V_{DF}=0.8V$ )



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### ◆CMOS

- ◆Highly Accurate :  $\pm 2\%$
- ◆Low Power Consumption :  $1.0\mu A$  ( $V_{IN} = 2.0V$ )
- ◆Ultra small Mini Mold Package

### ■Applications

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

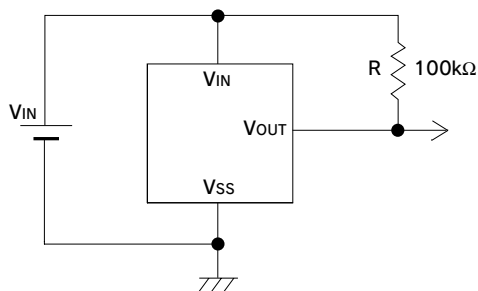
### ■General Description

The XC61A series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies. Detect voltage is extremely accurate with minimal temperature drift. N channel open drain output configurations is available.

### ■Features

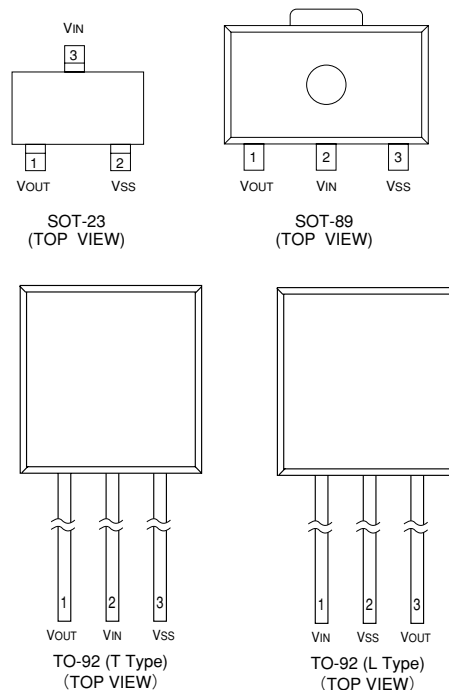
- Highly accurate** :  $\pm 2\%$
- Low power consumption**: TYP  $1.0\mu A$  [ $V_{IN}=2.0V$ ]
- Detect voltage range** :  $0.8V$  (N-ch open drain)
- Operating voltage range** :  $0.7V \sim 6.0V$
- Detect voltage temperature characteristics**  
: TYP  $\pm 100ppm/^{\circ}C$
- Output configuration** : N-channel open drain
- Ultra small package** : SOT-23 (150mW) mini-mold  
: SOT-89 (500mW) mini-mold  
: TO-92 (300mW)

### ■Typical Application Circuit



N-ch Open Drain Output

### ■Pin Configuration



### ■Pin Assignment

PIN NUMBER				PIN NAME	FUNCTION
SOT-23	SOT-89	TO-92 (T)	TO-92 (L)		
3	2	2	1	$V_{IN}$	Supply Voltage Input
2	3	3	2	$V_{SS}$	Ground
1	1	1	3	$V_{OUT}$	Output

## Product Classification

### Ordering Information

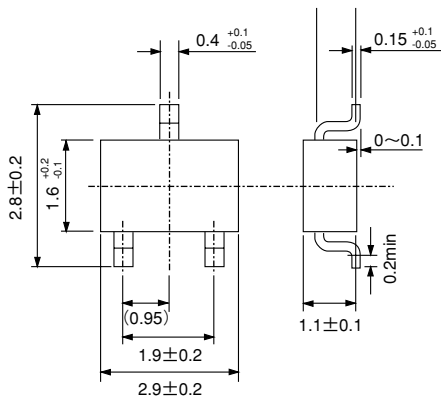
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DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	Output Configuration : N = N-ch open drain	e	Package Type : M = SOT-23 P = SOT-89 T = TO-92 ( regular ) L = TO-92 ( Custom pin Configuration)
b	Detect Voltage : 08 = 0.8V		
c	Output Delay : 0 = No delay	f	Device Orientation : R = Embossed Tape ( Right ) L = Embossed Tape ( Left ) H = Paper Tape (TO-92) B = Bag (TO-92)
d	Detect Accuracy : 2 = within $\pm 2.0\%$		

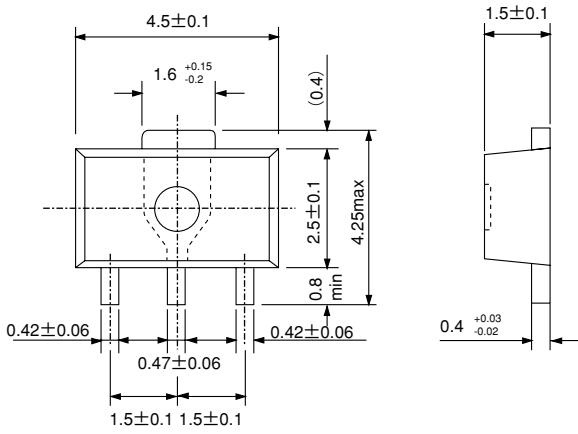
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## Packaging Information

### SOT-23

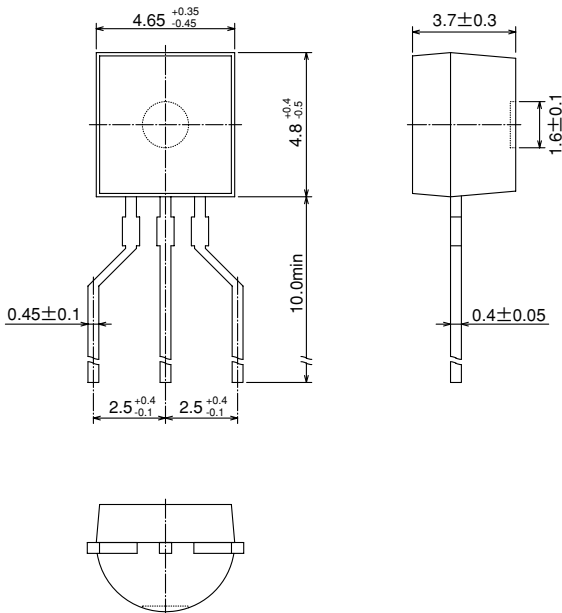


●SOT-89



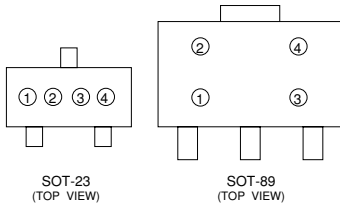
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●TO-92



## Marking

### ●SOT-23, SOT-89



① Represents the integer of the Output Voltage and Detect Voltage

DESIGNATOR	CONFIGURATION	VOLTAGE
K	N-ch	0.②(V)

② Represents the decimal point of the Detect Voltage

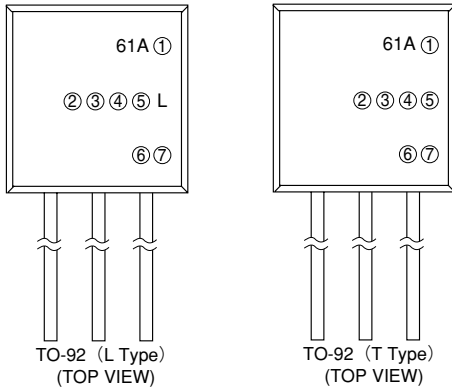
DESIGNATOR	VOLTAGE
8	①.8(V)

③ Indicates 'Delay Time'

DESIGNATOR	DELAY TIME
0	No Delay

④ Represents the assembly lot no.  
Based on internal standards

### ●TO-92



① Represents the output configuration

DESIGNATOR	OUTPUT CONFIGURATION
N	N-ch

② Represents the Detect Voltage

DESIGNATOR		VOLTAGE (V)
②	③	
0	8	0.8

④ Indicates Delay Time

DESIGNATOR	DELAY TIME
0	No delay

⑤ Represents the Detect Voltage Accuracy

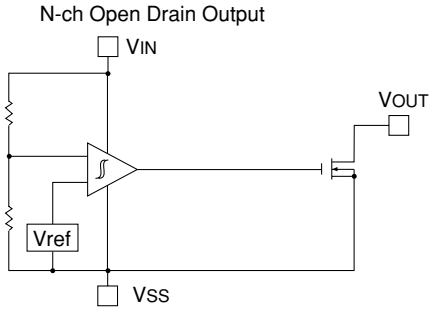
DESIGNATOR	DETECT VOLTAGE ACCURACY
2	within $\pm 2\%$

⑥ Represents a least significant digit of the produced year

DESIGNATOR	Produced year
0	2000
1	2001

⑦ Denotes the production lot number  
0 to 9, A to Z repeated(G.I.J.O.Q.W excepted)

## Block Diagram



## Absolute Maximum Ratings

Ta = 25°C

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	V <sub>IN</sub>	9	V
Output Current	I <sub>OUT</sub>	50	mA
Output Voltage	N-ch open drain V <sub>OUT</sub>	V <sub>SS</sub> -0.3 ~ 9	V
Power Dissipation	SOT-23	P <sub>d</sub>	150
	SOT-89		500
	TO-92		300
Operating Ambient Temperature	T <sub>opr</sub>	-30 ~ +80	°C
Storage Temperature	T <sub>stg</sub>	-40 ~ +125	°C

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## Electrical Characteristics

Ta = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Detect Voltage	V <sub>DF</sub>		V <sub>DF</sub> x 0.98	V <sub>DF</sub>	V <sub>DF</sub> x 1.02	V
Hysteresis Range	V <sub>HYS</sub>		V <sub>DF</sub> x 0.02	V <sub>DF</sub> x 0.05	V <sub>DF</sub> x 0.08	V
Supply Current	I <sub>SS</sub>	V <sub>IN</sub> = 1.5V		0.9	2.6	μA
		= 2.0V		1.0	3.0	
		= 3.0V		1.3	3.4	
		= 4.0V		1.6	3.8	
		= 5.0V		2.0	4.2	
Operating Voltage	V <sub>IN</sub>	V <sub>DF</sub> = 0.8V to 2.0V	0.7		6.0	V
Output Current	I <sub>OUT</sub>	N-ch V <sub>DS</sub> = 0.5V V <sub>IN</sub> = 0.7V = 1.0V		0.35 2.2		mA
Temperature Characteristics	$\frac{\Delta V_{DF}}{\Delta T_{opr} + V_{DF}}$	-30°C ≤ T <sub>opr</sub> ≤ 80°C		± 100		ppm/°C
Delay Time (V <sub>DR</sub> → V <sub>OUT</sub> inversion)	t <sub>DLY</sub>				0.2	ms

Note :

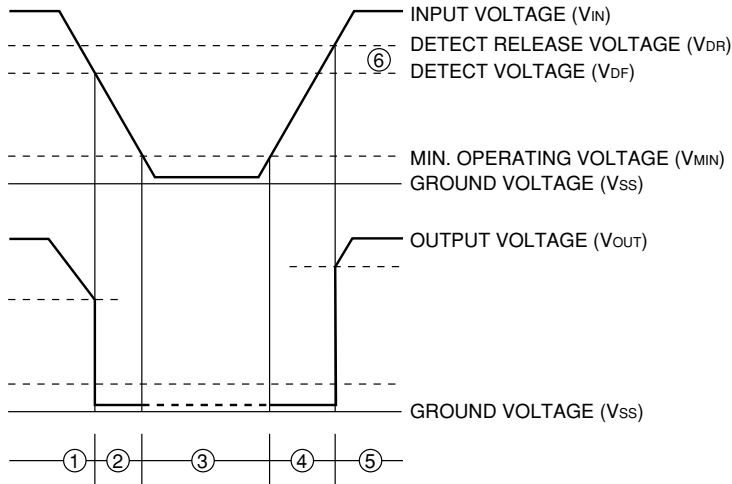
When a resistor is connected between the V<sub>IN</sub> pin and the input, V<sub>DR</sub> will increase and it may be the case that the established characteristics cannot be achieved.

## Functional Description

### Functional Description

- ① When input voltage ( $V_{IN}$ ) rises above detect voltage ( $V_{DF}$ ), output voltage ( $V_{OUT}$ ) will be equal to  $V_{IN}$ .  
( A condition of high impedance exists with Nch open drain output configurations. )
- ② When input voltage ( $V_{IN}$ ) falls below detect voltage ( $V_{DF}$ ), output voltage ( $V_{OUT}$ ) will be equal to the ground voltage ( $V_{SS}$ ) level.
- ③ When input voltage ( $V_{IN}$ ) falls to a level below that of the minimum operating voltage ( $V_{MIN}$ ), output will become unstable. In this condition,  $V_{IN}$  will equal the pulled-up output ( should output be pulled-up.)
- ④ When input voltage ( $V_{IN}$ ) rises above the ground voltage ( $V_{SS}$ ) level, output will be unstable at levels below the minimum operating voltage ( $V_{MIN}$ ). Between the  $V_{MIN}$  and detect release voltage ( $V_{DR}$ ) levels, the ground voltage ( $V_{SS}$ ) level will be maintained.
- ⑤ When input voltage ( $V_{IN}$ ) rises above detect release voltage ( $V_{DR}$ ), output voltage ( $V_{OUT}$ ) will be equal to  $V_{IN}$ .  
( A condition of high impedance exists with Nch open drain output configurations. )
- ⑥ The difference between  $V_{DR}$  and  $V_{DF}$  represents the hysteresis range.

### Timing Chart



## Directions for use

### Notes on Use

When a resistor is connected between the  $V_{IN}$  pin and the input with N-channel open drain output configurations, we suggest that a resistor with an  $R_{IN}$  value of less than  $1\text{k}\Omega$  and a capacitor with a value of more than  $0.1\mu\text{F}$  be used in order to avoid oscillation.

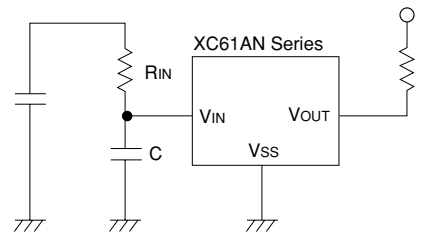


Diagram: Circuit using an input resistor